





EURO^{4SEE}

Optimizing Deep Learning Systems for Hardware Assoc. Prof. Erdem AKAGÜNDÜZ, METU







Pl.a : Why hardware matters in deep learning?

• Pl.b : Performance metrics

Pl.c : Case Study: Edge Devices vs Datacenter vs

Supercomputers





- Hardware is not universal; it is designed for specific types of computation.
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- Hardware is not universal; it is designed for specific types of computation.
- Different hardware handles different operations at different speeds.
- Some hardware excels at logic/branching, others at matrix math.
- For example:
 - Fixed-point vs floating-point computation: each hardware type is optimized differently.





- 1. Logic Operations
 - o AND, OR, XOR, NOT
 - o Bitwise operations
 - o Comparisons (>, <, ==)</pre>





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- 2. Branching / Control Flow
 - Conditional statements (if/else)
 - Loops with unpredictable iteration counts
 - o Function calls and returns





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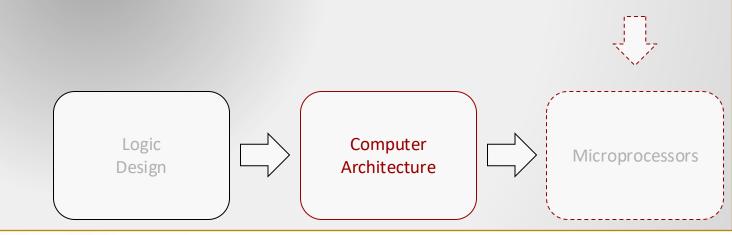
- 3. Memory Operations
 - o Read from memory / cache
 - o Write to memory / cache
 - o Load/store operations







- 4. Arithmetic Operations
 - Additions / Subtractions
 - Multiplications / Divisions
 - Floating-point vs fixed-point computation
 - Accumulations / reductions (sums, averages)







- 5. Specialized Vector / Matrix Operations
 - O Dot products, matrix multiplications
 - o Convolutions
 - Tensor contractions
 - o Batch operations

Co-processors

Logic Design



Computer Architecture



Microprocessors

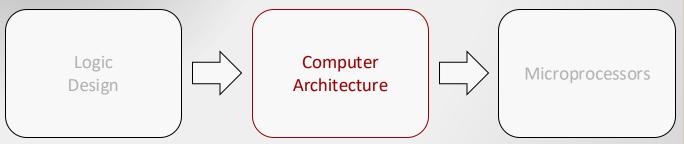




- 6. Miscellaneous / Specialized
 - Random number generation
 - Transcendental functions (exp, log, sin, cos)
 - Activation functions in neural networks
 - Parallelization
 - Quantization
 - o others...







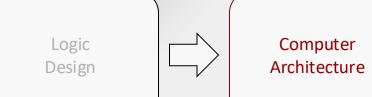




- Arithmetic-heavy:
 - o Matrix / vector operations:
 - Core of forward/backward passes (dense linear algebra)
 - o Reductions (sum/average):
 - Computing losses, gradients, normalization layers
 - O Multiplication / division / accumulation:
 - Weight updates, activations









Microprocessors





- Memory-heavy:
 - o Read/write/transfer:
 - Loading inputs, activations, weights; storing gradients
 - o Memory bandwidth:
 - which often becomes a limiting factor, especially for large models!

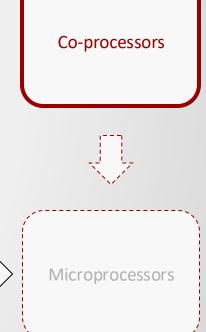
Co-processors







- Logic / branching:
 - Minimal in standard feed-forward neural nets
 - More significant in models with dynamic architectures, RNNs with variable lengths, or conditional execution
 - BP-thru-time in RNNs



Logic Design



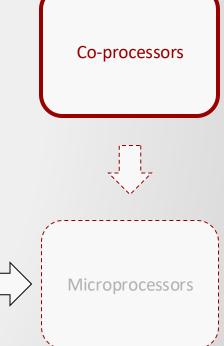
Computer Architecture







- Specialized functions:
 - Activation functions (ReLU, Sigmoid, GELU)
 - Softmax, normalization layers, random sampling (dropout)



Logic Design



Computer Architecture







- Training:
 - o Arithmetic-bound:
 - Most time spent in matrix multiplications for forward/backward passes
 - o Memory-bound:
 - Storing activations for backpropagation; transferring weights across devices in distributed setups
 - o Communication-bound:
 - In multi-GPU/HPC setups, gradient synchronization can be a bottleneck



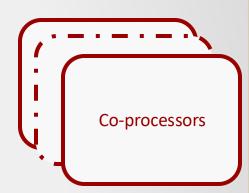
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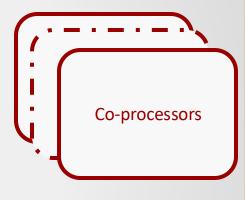
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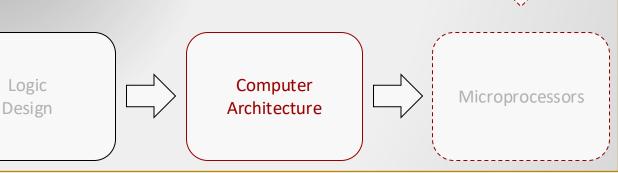






- Inference:
 - Arithmetic-bound for large models, but generally less intensive than training
 - Memory-bound if model is too large for cache/VRAM
 - o Latency-sensitive:
 - Especially for edge devices; you may optimize for lowlatency rather than max throughput

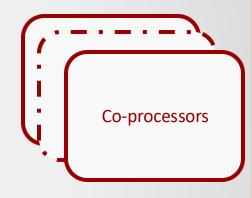








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latency? throughput?









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Thanks!





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